

Claims 1 through 13 are pending in this application. Independent claims 1 and 7 have been amended. Care has been exercised to avoid the introduction of new matter. Indeed, adequate descriptive support for the present Amendment should be apparent throughout the originally filed disclosure as, for example, as recognized by the Examiner, in the paragraph bridging pages 5 and 6 of the written description of the specification. Applicants submit that the present Amendment does not generate any new matter issue, or any new issue for that matter.

A clean copy of amended claims 1 and 7 appear in the Appendix hereto.

Claims 1 through 13 were rejected under the first paragraph 35 U.S.C. § 112 for lack of adequate descriptive support.

In the statement of the rejection, the Examiner asserted that the originally filed disclosure discloses that the plurality of connecting conductors penetrate the protective dielectric layer, but not the protective insulating layer which was considered to include the sealing resin and coating layer. This rejection is traversed.

In response, independent claims 1 and 7 have been amended to clarify that the plurality of connecting conductors penetrate the coating layer, noting element 7 in Fig. 1, thereby overcoming the stated basis for the imposed rejection. Accordingly, withdrawal of the rejection of claims 1 through 13 under the first paragraph of 35 U.S.C. § 112 for lack of adequate descriptive support is solicited.

Claims 7 through 10 were rejected under 35 U.S.C § 103 for obviousness predicated upon the acknowledged prior art in view of Ohtsuka et al. and Omoya et al.

This rejection is traversed.

Violation of due process of law.

It is fundamental that Applicants are entitled to a response to their arguments. In the responsive Amendment submitted April 8, 2002, and in the Request for Reconsideration submitted September 12, 2002, Applicants argued that Ohtsuka et al. do not teach or disclose a connecting member having a plurality of layers. Ohtsuka et al. merely disclose a plurality of diffusion barriers within a protective dielectric layer. In accordance with the semiconductor device defined in claim 7, the connecting conductors extend beyond the outer surface of the protective insulating layer which comprises a coating layer which covers the surface of the semiconductor chip. This being the case, it is **not** apparent and the Examiner has **not** explained **why** one having ordinary skill in the art would have been realistically impelled to modify the Fig. 3 device by providing a plurality of layers of different material to form the connecting conductor, merely because of the diffusion barriers disclosed by Ohtsuka et al. are within the protective insulating layer. *In re Rouffet*, 149 F.3d 1350, 47 USPQ2D 1453 (Fed Cir. 1998).

To whatever extent the Examiner is relying upon the doctrine of inherency, such reliance is misplaced for lack of certainty in concluding that one of the layers would necessarily reduce stress and in confusing obviousness with inherency. *In re Rijckaert, supra*; *In re Shetty, supra*. Moreover, the **problem** addressed and solved by the claimed invention, i.e., stresses caused by a difference in coefficients of linear expansion between the semiconductor chip and sealing resin, is not recognized or addressed by the applied prior art. *Jones v. Hardy*, 727 F.2 1524, 220 USPQ 1021 (Fed. Cir. 1984).

The Examiner cannot sit back and ignore the arguments advanced by Applicants without giving Applicants the courtesy of a response. Indeed, this is more than a courtesy; this is the Examiner's obligation, because the Examiner cannot leave Applicants in the unenviable position

of shooting arrows into the dark attempting to guess on how the Examiner is viewing the arguments. *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

Based upon the above arguments, which are **again** advanced for the Examiner's consideration, Applicants submit that a *prima facie* basis to deny patentability to the claimed invention has not been established. Moreover, upon giving due consideration to the problem addressed and solved by the claimed invention, which is not even the radar screen of the applied references, the conclusion appears inescapable that one having ordinary skill in the art would **not** have found the claimed invention **as a whole** obvious within the meaning of 35 U.S.C. § 103.

Jones v. Hardy, supra.

Applicants, therefore, submit that the imposed rejection of claims 7 through 10 under 35 U.S.C. § 103 for obviousness predicated upon the acknowledged prior art in view of Ohtsuka et al. and Omoya et al. is not factually or legally viable and, hence, solicit withdrawal thereof.

Claims 11 through 13 were rejected under 35 U.S.C. § 103(a) for obviousness predicated upon the acknowledged prior art in view of Ohtsuka et al., Omoya et al., Matsumoto et al. and Chakravorty.

This rejection is traversed. Claims 11 through 13 depend from independent claim 7. Applicants incorporate herein the arguments previously advanced in traversing the imposed rejection of claim 7 under 35 U.S.C. § 103 for obviousness predicated upon the acknowledged prior art of Ohtsuka et al. and Omoya et al. The additional references to Matsumoto et al. and Chakravorty do not cure the argued deficiencies in the attempted basic combination of the acknowledged prior art, Ohtsuka et al. and Omoya et al.

Moreover, Applicants separately argue the patentability of claims 11 through 13. Specifically, Further, Matsumoto et al. do not relate to connective conducting layers but merely to an interconnect pattern defining internal circuitry. It is not apparent and the Examiner has not explained why one having ordinary skill in the art would somehow been realistically motivated to modify the single connecting conductor of the Fig. 3 device by forming a plurality of staggered layers of different material, merely because of the conventionality of an interconnection pattern disclosed by Matsumoto et al. which does not relate to a connecting conductor to a bump external terminal. Further, as also previously argued, the applied art neither recognizes nor addresses the cracking problem addressed and solved by the claimed invention.

The additional reference to Chakravorty is of no avail. Reference numeral 311 identifies an underbump layer which merely provides electrical connection to trace 307 which is connected to contact pad 304 on the chip. The actual bump layer is designated by reference numeral 314 (Fig. 8d). The Examiner has not pointed out wherein Chakravorty discloses or suggests the concept of providing a layer having reduced hardness for any purpose, let alone for stress relief, as in the claimed invention.

It should, therefore, be apparent that a prima facie basis to deny patentability to the claimed invention has **not** been established. Further, upon considering the **problem** addressed and solved by the claimed invention as a potent indicium of **nonobviousness**, Applicants submit that one having ordinary skill in the art would **not** have found the claimed invention **as a whole** within the meaning of 35 U.S.C. §103. *Jones v. Hardy, supra*.

Applicants, therefore, submit that the imposed rejection of claims 11 through 13 under 35 U.S.C. §103 for obviousness predicated upon the acknowledged prior art (Fig. 3) in view of

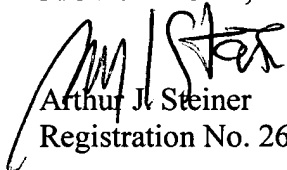
Ohtsuka et al., Omoya et al., Matsumoto et al., and Chakravorty is not factually or legally viable and, hence, solicit withdrawal thereof.

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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